Notice of Allowability	Application No.	Applicant(s)	
	10/039,585	CHEN, HONGYI· HUBERT	
	Examiner	Art Unit	
	Esaw T. Abraham	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amdt filed on 06/20/05*.

2. ☒ The allowed claim(s) is/are *1-80*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

Examiner's statement for reason for allowance

1. Claims **8-12, 14, 16, 18 and 67-76** have been previously allowed.

2. Claims **1-7, 13, 15, 17, 19-66, and 77-80** have been allowed.

The following is an examiner's statement for allowance:

As per claim 1:

The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination creating a circuit comprising a plurality of registers wherein each of the plurality or registers is associated with a corresponding logic gate; and programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero, wherein the step of programming is based on a pre-selected polynomial key word. Consequently, claim 1 is allowed over the prior art.

Claims **4-7 and 60,** which is/are directly or indirectly dependent/s of claim 1 are also allowable over the prior art of record.

As per claim 2:

The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination creating a circuit comprising a plurality of registers wherein each of the plurality or registers is associated with a corresponding logic gate; and programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero, wherein the step of programming is based on a pre-selected polynomial key word wherein programming comprises programming a first set of selection inputs, wherein: the step of programming the first set of selection inputs is based on the

pre-selected polynomial key word; the first set of selection inputs is associated with: selecting corresponding input from each of the logic gates; and a shift logic that is associated with the plurality of registers. Consequently, claim 2 is allowed over the prior art.

As per claim 3:

The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination creating a circuit comprising a plurality of registers wherein each of the plurality or registers is associated with a corresponding logic gate; and programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero, wherein the step of programming is based on a pre-selected polynomial key word wherein the step of programming comprises: programming a second set of selection inputs, wherein the second set of selection inputs is associated with selecting corresponding input to each of the logic gates; the second set of selection inputs is associated with the selecting a final output from among output from the plurality of registers; and the step of programming the second set of selection inputs is based on the pre-selected polynomial key word. Consequently, claim 3 is allowed over the prior art.

As per claim 13:

The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero, wherein the step of programming is based on a pre-selected polynomial key word. Consequently, claim 13 is allowed over the prior art.

As per claim 15:

The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination creating a circuit comprising means for creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and means for programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero, wherein the step of programming is based on a pre-selected polynomial key word. Consequently, claim 15 is allowed over the prior art.

As per claim 17:

The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination creating a circuit comprising means for creating a circuit comprising a processor; one or more stored sequences of instructions which, when executed by the processor, cause the processor to carry out the steps of: creating a circuit comprising a plurality of registers wherein each of the plurality of registers is associated with a corresponding logic gate; and programming a subset of the plurality of registers to have a value of zero and programming a corresponding subset of the logic gates to have a value of zero, wherein the step of programming is based on a pre-selected polynomial key word. Consequently, claim 17 is allowed over the prior art.

As per claim 19:

The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination creating a circuit comprising a first set of N storage elements, wherein a first selection signal is configured to select a subset of the first set of N storage

elements, and wherein each storage element of the subset of the first set of N storage elements corresponds to a term of a pre-selected CRC polynomial keyword; and M logic circuits, wherein an input of each of the M logic circuits is in communication with an output of a corresponding one of the first set of N storage elements, and wherein a second selection signal is configured to select an output of one storage element of the subset of the first set of N storage elements corresponding to a length of the pre-selected CRC polynomial keyword. Consequently, claim 19 is allowed over the prior art.

Claims **20-30, 61 and 62,** which is/are directly or indirectly dependent of claim 19 are also allowable over the prior art of record.

As per claim 31:

The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination generating CRC codes comprising first set of N means for storing data, wherein a first selection signal is configured to select a subset of the first set of N data storing means, and wherein each data storing means of the subset of the first set of N data storing means corresponds to a term of a pre-selected CRC polynomial keyword; and M logic circuit means, wherein an input of each of the M logic circuit means is in communication with an output of a corresponding one of the first set of N data storing means, and wherein a second selection signal is configured to select an output of one data storing means of the subset of the first set of data storing means corresponding to a length of the pre-selected CRC polynomial keyword. Consequently, claim 31 is allowed over the prior art.

Claims **32-42, 63 and 64,** which is/are directly or indirectly dependent of claim 31 are also allowable over the prior art of record.

As per claim 43:

The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination generating CRC codes comprising storing a first signal N times logically combining each stored first signal with one of an input signal and a selected signal M times; selecting a subset of the N storing steps in response to a first selection signal, wherein each storing step of the subset of the N storing steps corresponds to a term of a pre-selected CRC polynomial; and selecting an output of one storing step of the subset of N storing steps corresponding to a length of the pre-selected CRC polynomial keyword, in response to a second selection signal. Consequently, claim 43 is allowed over the prior art.

Claims **44-51 and 65,** which is/are directly or indirectly dependent of claim 43 are also allowable over the prior art of record.

As per claim 52:

The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination generating CRC codes comprising controlling storing of a first signal N times; logically combining each stored first signal with one of an input signal and a selected signal M times; providing a first selection signal to select a subset of the N storing steps, wherein each storing step of the subset of the N storing steps corresponds to a term of a' pre-selected CRC polynomial; and providing a second selection signal to select an output of one storing step of the subset of N storing steps corresponding to a length of the pre-selected CRC polynomial keyword. Consequently, claim 52 is allowed over the prior art.

Claims **53-59 and 66,** which is/are directly or indirectly dependent of claim 52 are also allowable over the prior art of record.

As per claim 77:

The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination generating CRC codes comprising shifting a first signal N times, exclusive or'ing each shifted first signal with one of an input signal and a selected signal M times; selecting one of an output of a corresponding one of the M exclusive or'ing steps and an output of a corresponding one of the N storing steps, in response to a first selection signal, wherein an input of an nth one of the N shifting steps is in communication with an output of an n-1th one of the N selecting steps of step (c); selecting, M times, one of an output of a first subset of the N storing steps and an output of a second subset of the N storing steps, in response to a second selection signal, wherein a first input of an mth one of the selecting steps of step (d) is in communication with an output of an m+lth one of the selecting steps of step (d), and wherein a second input of the mth one of the selecting steps of step (d) is in communication with an output of an nth one of the selecting steps of step (c); selecting, M times, one of an output of step (d) and an input signal to form the selected signal, in response to the second selection signal; selecting a subset of the N storing steps in response to the first selection signal, wherein each storing step of the subset of the N storing steps corresponds to a term of a pre-selected CRC polynomial; and selecting an output of one storing step of the subset of N storing steps corresponding to a length of the pre-selected CRC polynomial keyword as the output of the pre-selected CRC polynomial keyword, in response to the second selection signal. Consequently, claim 77 is allowed over the prior art.

Claim **78,** which is/are directly or indirectly dependent of claim 77 is also allowable over the prior art of record.

As per claim 79:

The prior art of record teaches the claimed invention substantially, but it fails to teach or suggest singly or in combination controlling shifting of a first signal N times, exclusive or'ing each shifted first signal with one of an input signal and a selected signal M times; providing a first selection signal to select one of an output of a corresponding one of the M exclusive or'ing steps and an output of a corresponding one of the N storing steps, wherein an input of an nth one of the N shifting steps is in communication with an output of an n-lth one of the N selecting of step; providing a second selection signal to select, M times, one of an output of a first subset of the N storing steps and an output of a second subset of the N storing steps, wherein a first input of an mth one of the selecting of step is in communication with an output of an m+lth one of the selecting of step, and wherein a second input of the mth one of the selecting of step is in communication with an output of an nth one of the selecting of step providing the second selection signal to select, M times, one of an output of the selecting of step and an input signal to form the selected signal; providing the first selection signal to select a subset of the N storing steps, wherein each storing step of the subset of the N storing steps corresponds to a term of a pre-selected CRC polynomial; and providing the second selection signal to select an output of one storing step' of the subset of N storing steps corresponding to a length of the pre-selected CRC polynomial keyword as the output of the pre-selected CRC polynomial keyword. Consequently, claim 79 is allowed over the prior art.

Claim **80,** which is/are directly or indirectly dependent of claim 79 is also allowable over the prior art of record.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

3. Any inquiry concerning this communication or earlier communication from the examiner should be directed to Esaw Abraham whose telephone number is (571) 272-3812. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are successful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone numbers for the organization where this application or proceeding is assigned (571) 273-8300.

Information regarding the status of an Application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or PUBLIC PAIR. Status information for unpublished applications is available through Private Pair only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Art unit: 2133

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